

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
REQUEST FOR FILING NATIONAL PATENT APPLICATION
Under 35 USC 111(a) and Rule 53(b)

Jc59 U.S. PTO
03/30/99 01/28/00


Asst. Commissioner of Patents
Washington, D.C. 20231

jc685 U.S. PTO



01/28/00

Sir:

WITH SIGNED DECLARATION

PATENT APPLICATION

NONPROVISIONAL
NON REISSUE
NON PCT NAT PHASE

Herewith is the PATENT APPLICATION of
Inventor(s): SHIBATA, Naoki

Title GROUP III NITRIDE COMPOUND SEMICONDUCTOR
DEVICE

Atty. Dkt.: PM 266204 T36-119817M/KOH
M# Client Ref

including:

Date: January 28, 2000

1. Specification: 16 pages (only spec. and claims) 2. Specification in non-English language
3. Declaration Original Facsimile/Copy Abstract 1 page(s); 6 numbered claims
4. Drawings: 3 sheet(s) informal; formal of size: A4 11"
5. See top first page re prior Provisional, National or International application(s). ("X" box only if info is there and do not complete corresponding item 5 or 6). (Prior M# _____ SN _____)
6. AMD**N**E the specification please by inserting before the first line: -- This is a Continuation-in-Part
 Divisional Continuation Substitute Application (MPEP 201.09) of:
(a) National Appln. No. _____ / filed _____ (M# _____)
(b) International Appln. No. _____ / filed _____
7. AMD**N**E the specification by inserting before the first line: -- This application claims the benefit of U.S. Provisional Application No. 60/_____, filed _____
8. Attached is an assignment and cover sheet. Please return the recorded assignment to the undersigned.
9. Prior application is assigned to _____

by Assignment recorded _____ Reel _____ Frame _____

10. FOREIGN priority is claimed under 35 USC 119(a)-(d)/365(b) based on filing in JAPAN

11. (country)

Application No.	Filing Date	Application No.	Filing Date
(1) 11-065880	12 MAR 1999	(2)	
(3)		(4)	
(5)		(6)	
(7)		(8)	
(9)		(10)	

12. (No.) Certified copy (copies): attached; previously filed (date) _____
in U.S. Application No. _____ / filed on _____

13. Attached: _____ (No.) Verified Statement(s) establishing "small entity" status under Rules 9 & 27.

14. **DOMESTIC/INTERNATIONAL** priority is claimed under 35 USC 119(e)/120/365(c) based on the following provisional, nonprovisional and/or PCT international application(s):

Application No.	Filing Date	Application No.	Filing Date
(1)		(4)	
(2)		(5)	
(3)		(6)	

15. This application is being filed under Rule 53(b)(2) since an inventor is named in the enclosed Declaration who was not named in the prior application.

16. Attached:

17. Preliminary Amendment:

THE FOLLOWING FILING FEE IS BASED ON CLAIMS AS FILED LESS ANY ABOVE CANCELLED

18. Basic Filing Fee	Large/Small Entity	Fee Code
19. Total Effective Claims 6 minus 20 = *0	\$690/\$345 x \$18/\$9 = + 0	101/201 103/203
20. Independent Claims 2 minus 3 = *0	x \$78/\$39 = + 0	102/202
21. If any proper multiple dependent claim (ignore improper) is present , add (Leave this line blank if this is a reissue application)	+ \$260/\$130 *If answer is zero or less, enter "0"	+ 0 104/204
22. TOTAL FILING FEE ENCLOSED =	\$690	
23. If "non-English" box 2 is X'd, add Rule 17(k) processing fee	+ \$130	+ 0 139
24. If "assignment" box 8 is X'd, add recording fee	+ \$40	+ 40 581
25. <input type="checkbox"/> Attached is a Petition/Fee under Rule No.	+ \$130	+ 0 122
26. Our Deposit Account No. 03-3975 Our Order No. 51273 C# 266204 MF# _____	TOTAL FEE ENCLOSED =	\$730

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Pillsbury Madison & Sutro LLP
Intellectual Property Group

1100 New York Avenue, NW
Ninth Floor
Washington, DC 20005-3918
Tel: (202) 861-3000
PWG/sdm

By Atty: Peter W. Gowdey

Reg. No. 25872

Sig:

Peter W. Gowdey 1/1/98

Fax: (202) 822-0944

Tel: (202) 861-3078

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APPLICATION UNDER UNITED STATES PATENT LAWS

Atty. Dkt. No. PM 266204
(M#)

Invention: GROUP III NITRIDE COMPOUND SEMICONDUCTOR DEVICE

Inventor (s): SHIBATA, Naoki

Pillsbury Madison & Sutro LLP
Intellectual Property Group
1100 New York Avenue, NW
Ninth Floor
Washington, DC 20005-3918
Attorneys
Telephone: (202) 861-3000

This is a:

- Provisional Application
- Regular Utility Application
- Continuing Application
- PCT National Phase Application
- Design Application
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- Plant Application
- Substitute Specification
Sub. Spec Filed
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SPECIFICATION

GROUP III NITRIDE COMPOUND SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

1. Field of Invention

5 The present invention relates to a group III nitride compound semiconductor device.

The present application is based on Japanese Patent Application No. Hei. 11-65880, which is incorporated herein by reference.

10 2. Description of the Related Art

It is known that group III nitride compound semiconductors can be utilized, for example, as blue light-emitting devices. As a method of producing a group III nitride compound semiconductor device, there has been heretofore

15 proposed a method comprising the steps of: growing a buffer layer of AlN or GaN on a sapphire substrate; growing a layer of GaN or AlGaN (hereinafter referred to as undercoat layer) by several microns on the buffer layer; and growing a layer of InGaN (hereinafter referred to as InGaN layer) on the undercoat 20 layer (see Japanese Patent No. 2751963).

In the aforementioned method, however, the composition of the InGaN layer was different from the composition of the undercoat layer (AlGaN or GaN). Hence, the former was heteroepitaxially grown on the latter. Moreover, when the two 25 layers were to be formed by means of a metal organic chemical vapor deposition method (hereinafter abbreviated as MOCVD method), the temperature for the growth of the undercoat layer (AlGaN or GaN) was generally about 1000°C whereas the

temperature for the growth of the InGaN layer was from about 700°C to about 900°C. Improvement in crystallinity of the InGaN layer formed on the undercoat layer was limited because of the problem in heteroepitaxial growth and difference between the 5 growth temperatures as described above.

SUMMARY OF THE INVENTION

Therefore, the present invention has as its object the provision of a novel-structure of a group III nitride compound 10 semiconductor device having an InGaN layer higher in crystallinity. By improvement in crystallinity of InGaN, improvement in emitted light intensity is attained when InGaN is utilized for a light-emitting device.

The present invention is designed to solve the 15 aforementioned problem. According to a first aspect of this invention, the configuration is as follows. That is,

According to the semiconductor device configured in the aforementioned manner, the second layer of $In_yGa_{1-y}N$ ($0 < y < 1$, $y \neq x$) is constituted by the same composition as the first layer 20 of $In_xGa_{1-x}N$ ($0 < x < 1$) which is the undercoat of the second layer. Hence, not only the second layer can be homoepitaxially grown on the first layer but also the two layers can be grown at substantially equal growth temperatures. As a result, the second layer high in crystallinity can be obtained.

25 Features and advantages of the invention will be evident from the following detailed description of the preferred embodiments described in conjunction with the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings:

Fig. 1 is a sectional view showing a light-emitting diode 1 as an embodiment of the present invention;

5 Fig. 2 is an enlarged sectional view of important part of a light-emitting diode 10 as another embodiment of the present invention;

10 Fig. 3 is an enlarged view of important part of a light-emitting diode 20 as a further embodiment of the present invention;

15 Fig. 4 is a sectional view showing a light-emitting diode 30 as a further embodiment of the present invention;

Fig. 5 is an enlarged view of important part of a light-emitting diode 40 as a further embodiment of the present invention; and

20 Fig. 6 is an enlarged view of important part of a light-emitting diode 50 as a further embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Respective constituent elements of the present invention will be described below.

A group III nitride compound semiconductor is generally represented by $\text{Al}_x\text{Ga}_y\text{In}_{1-x-y}\text{N}$ ($0 \leq x \leq 1$, $0 \leq y \leq 1$, $x+y \leq 1$). A layer of such a GaN semiconductor is grown by the known MOCVD method. Alternatively, the layer can be grown by a known molecular beam epitaxy method (hereinafter abbreviated as MBE method), or the like.

The substrate used in the present invention is optional. A sapphire substrate is used preferably. Besides this, substrates of Si, SiC, etc. can be used.

When a sapphire substrate is used, $\text{Al}_x\text{Ga}_{1-x}\text{N}$ ($0 \leq x \leq 1$) is used as a buffer layer. The buffer layer is used for facilitating the formation of the GaN semiconductor layer. The thickness of the buffer layer is not limited specially. Further, the buffer layer may be provided as a single layer or as a laminate consisting of a plurality of buffer layers.

Also when another substrate material is used, a buffer layer of a material adapted for the substrate material is used. When, for example, an Si (111) substrate is adopted, a buffer layer having a structure of Al/TiN/Ti viewed from the substrate side is used.

The first layer is formed of $\text{In}_x\text{Ga}_{1-x}\text{N}$ ($0 < x < 1$). When, for example, the first layer is used as a clad layer in a light-emitting device, the first layer is doped with an acceptor or a donor in order to obtain a desired electric conduction type.

Assuming now that $\text{Al}_x\text{Ga}_{1-x}\text{N}$ ($0 \leq x \leq 1$) is used as the buffer layer, the lattice constant of the buffer layer is smaller than the lattice constant of the first layer. Further, the difference between the lattice constants of the two layers decreases as the composition ratio of In in the first layer decreases. Therefore, the composition ratio of In in the first layer is preferably enlarged continuously or intermittently in the direction toward the second layer side from the buffer layer side. Consequently, not only the first layer in a face touching the buffer layer is lattice-matched with the buffer layer more

sufficiently but also the composition of the first layer in a face touching the second layer is made substantially equal to the composition of the second layer. In this manner, the first layer lattice-matched with the buffer layer in a first layer 5 face touching the buffer layer and lattice-matched with the second layer in a first layer face touching the second layer is obtained. As a result, the crystallinity of the first layer is improved, so that the quality of the second layer formed on the high-crystallinity first layer becomes higher.

10 Assuming now that the MOCVD method is taken as an example, the composition of the first layer can be changed continuously or intermittently only if the composition ratio of raw-material gases is changed continuously or intermittently in accordance with the growth of the first layer.

15 The second layer is formed of $In_xGa_{1-x}N$ ($0 < y < 1$, $y \neq x$). When, for example, this layer is used in a light-emitting device, this layer serves as a light-emitting layer. A known double hetero-structure, a known superlattice structure, or the like, is used as the light-emitting device. Moreover, the second 20 layer can be applied also to an electronic device represented by an FET structure.

Assuming now that a light-emitting device is taken as an example, a clad layer is formed on the second layer by a known method. When an electrically insulating substrate such as a 25 sapphire substrate, or the like, is used, an n-type electrode and a p-type electrode are formed after required etching steps.

Configuration according to a second aspect of the present invention will be described below. According to the aspect of

the present invention, the first layer according to the first aspect of the present invention is replaced by that of $\text{Al}_a\text{Ga}_b\text{In}_{1-a-b}\text{N}$ ($0 < a < 1$, $0 < b < 1$, $a+b < 1$). This is because addition of Al to the composition makes it possible to widen the band gap of the first layer compared with that according to the first aspect of the present invention. In this manner, when, for example, the second layer is used as a light-emitting layer in a light-emitting device, the role of a more excellent clad layer can be given to the first layer.

10 Although the composition ratio of Al and In in the first layer is optional, the composition ratio of Al and In is preferably selected so that the lattice constant of the first layer is made substantially equal to the lattice constant of the second layer in order to perform lattice matching between
15 the first layer and the second layer formed on the first layer.

Similarly to the case according to the first aspect of the present invention, the composition ratio of Al and In in the first layer may be changed continuously or intermittently in the direction toward the second layer side from the buffer
20 layer side. In this manner, the first layer more effectively lattice-matched with the buffer layer in a first layer face touching the buffer layer and lattice-matched with the second layer in a first layer face touching the second layer is obtained. As a result, the crystallinity of the first layer is improved,
25 so that the quality of the second layer formed on the high-crystallinity first layer becomes higher.

When the composition ratio of Al and In in the first layer is to be changed, the composition ratio of Al and In is preferably

changed so that the band gap of the first layer in a face touching the second layer becomes wider than the band gap of the second layer.

The aforementioned first layer is formed by the same method as that according to the first aspect of the present invention.

Embodiments according to the first aspect of the present invention will be described below with reference to the drawings.

10 FIRST EMBODIMENT

Fig. 1 shows a light-emitting diode 1 as an embodiment of the present invention. Specifications of respective semiconductor layers are as follows.

Layer	Component	Dopant	(Thickness)
p-type clad layer 6	p-GaN	Mg	(0.3 μ m)
Second layer: light-emitting layer 5	In _{0.15} Ga _{0.85} N		(3.5 nm)
First layer: n-type clad layer 4	n-In _{0.02} Ga _{0.98} N	Si	(4 μ m)
Buffer layer 3	AlN		(50 nm)
Substrate 2	sapphire		(300 μ m)

The buffer layer 3 is laminated on the substrate 1 by the MOCVD method.

The n-type clad layer 4, which is the first layer, may be of a double-layered structure with an n⁻ layer of a low electron density on the light-emitting layer 5 side and an n⁺ layer of a high electron density on the buffer layer 3 side.

20 The light-emitting layer 5, which is the second layer, is not limited to this embodiment but a multiple quantum well structure, or the like, can be used as this layer.

An Al_xGa_yIn_{1-x-y}N ($0 \leq x \leq 1$, $0 \leq y \leq 1$, $x+y \leq 1$) layer, which has

a wide band gap and which is doped with an acceptor such as magnesium, or the like, may be interposed between the light-emitting layer 5 and the p-type clad layer 6. This technique is employed for preventing electrons implanted into
5 the light-emitting layer 5 from being diffused into the p-type clad layer 6.

The p-type clad layer 6 may be of a double-layered structure with a p⁻ layer of a low hole concentration on the light-emitting layer 5 side and a p⁺ layer of a high hole
10 concentration on the electrode 7 side.

The Al_xGa_yIn_{1-x-y}N ($0 \leq x \leq 1$, $0 \leq y \leq 1$, $x+y \leq 1$) may be replaced for the light-emitting layer 5 instead of InGaN.

The respective semiconductor layers on the buffer layer
3 are formed by means of the known MOCVD method. In this growth
15 method, an ammonia gas and gases of group III metal alkyl compounds such as trimethylgallium (TMG), trimethylaluminum (TMA) and trimethylindium (TMI) are supplied onto a substrate heated to an appropriate temperature and are subjected to a thermal decomposition reaction to thereby grow a desired
20 crystal on the substrate.

After the p-type clad layer 6 is formed, the p-type clad layer 6, the light-emitting layer 5 and the n-type clad layer 4 are partially etched. Then, an n-type electrode 9 is formed on the n-type clad layer 4 by means of vapor deposition.

A light-transmissible electrode 7, which is constituted by a thin film containing gold, is laminated to cover the substantially whole area of an upper face of the p-type clad layer 6. A p-type electrode 8, which is constituted also by

a material containing gold, is formed on the light-transmissible electrode 7 by means of vapor deposition. Further, if the light-transmissible electrode 7 is constituted by a thick film, a light-emitting device of the type of
5 reflecting emitted light and taking-out light from the transparent sapphire substrate 2 may be provided.

SECOND EMBODIMENT

Fig. 2 shows an enlarged view of important part of a light-emitting diode 10 as another embodiment of the present
10 invention. Incidentally, the same members as used in the light-emitting diode 1 in the first embodiment are referred to by the same characters and the description thereof will be omitted.

In the light-emitting diode 10, the composition of an
15 n-type clad layer 14 is changed continuously from n-In_{0.01}Ga_{0.99}N (doped with Si) to n-In_{0.15}Ga_{0.85}N (doped with Si) in the direction toward the light-emitting layer 5 from the buffer layer 3. In the light-emitting diode 10, the composition ratio of In of the n-type clad layer becomes small on the buffer layer 3 side.
20 Hence, the difference between the lattice constant of the n-type clad layer and the lattice constant of the buffer layer 3 is reduced, so that the crystallinity of the n-type clad layer 14 is improved. Further, the composition ratio of In of the n-type clad layer 14 becomes substantially equal to that in the
25 light-emitting layer 5, on the light-emitting layer 5 side. Hence, the lattice constant of the n-type clad layer 14 becomes substantially equal to that of the light-emitting layer 5. Accordingly, the crystallinity of the light-emitting layer 5

is also improved.

When the MOCVD method is used for the formation of the n-type clad layer 14, the composition ratio of raw-material gases is changed continuously. In this manner, the n-type clad layer 14 having the composition changed continuously in the direction toward the light-emitting layer 5 side from the buffer layer 3 side is obtained.

THIRD EMBODIMENT

Fig. 3 shows an enlarged view of important part of a
10 light-emitting diode 20 as a further embodiment of the present invention. Incidentally, the same members as used in the light-emitting diode 1 in the first embodiment are referred to by the same characters and the description thereof will be omitted.

15 In the light-emitting diode 20, the composition of an n-type clad layer 24 is changed to three stages of $n\text{-In}_{0.02}\text{Ga}_{0.98}\text{N}$ (doped with Si), $n\text{-In}_{0.08}\text{Ga}_{0.92}\text{N}$ (doped with Si) and $n\text{-In}_{0.15}\text{Ga}_{0.85}\text{N}$ (doped with Si) in the direction toward the light-emitting layer 5 from the buffer layer 3. In the light-emitting diode 20, the
20 composition ratio of In of the n-type clad layer 24 becomes small on the buffer layer 3 side. Hence, the difference between the lattice constant of the n-type clad layer 24 and the lattice constant of the buffer layer 3 is reduced, so that the crystallinity of the n-type clad layer 24 is improved. Further,
25 the composition ratio of In of the n-type clad layer 24 becomes substantially equal to that in the light-emitting layer 5, on the light-emitting layer 5 side. Hence, the lattice constant of the n-type clad layer 24 becomes substantially equal to that

of the light-emitting layer 5. Accordingly, the crystallinity of the light-emitting layer 5 is also improved.

When the MOCVD method is used for the formation of the n-type clad layer 24, the composition ratio of raw-material gases is changed stepwise. In this manner, the n-type clad layer 24 having the composition changed stepwise in the direction toward the light-emitting layer 5 side from the buffer layer 3 side is obtained.

Although this embodiment has shown the case where the composition of the n-type clad layer 24 is changed to three stages, the present invention is not limited to the three-stage change.

Embodiments according to the second aspect of the present invention will be described below with reference to the drawings.

FOURTH EMBODIMENT

Fig. 4 shows a light-emitting diode 30 as an embodiment of the present invention. Incidentally, the same members as used in the light-emitting diode 1 in the first embodiment are referred to by the same characters and the description thereof will be omitted.

In the light-emitting diode 30, an n-type clad layer 34 is formed of $n\text{-Al}_{0.11}\text{Ga}_{0.61}\text{In}_{0.28}\text{N}$ (doped with Si). The thickness of the n-type clad layer 34 is 4 μm . Addition of Al to the composition makes it possible to widen the band gap of the n-type clad layer 34. Hence, the n-type clad layer 34 has the role of a barrier layer to holes overflowed from the light-emitting layer 5.

FIFTH EMBODIMENT

Fig. 5 shows an enlarged view of important part of a light-emitting diode 40 as another embodiment of the present invention. Incidentally, the same members as used in the 5 light-emitting diode 1 in the first embodiment are referred to by the same characters and the description thereof will be omitted.

In the light-emitting diode 40, the composition of an n-type clad layer 44 is changed continuously from n-
10 $\text{Al}_{0.34}\text{Ga}_{0.33}\text{In}_{0.33}\text{N}$ (doped with Si) to n- $\text{Al}_{0.11}\text{Ga}_{0.61}\text{In}_{0.28}\text{N}$ (doped with Si) in the direction toward the light-emitting layer 5 from the buffer layer 3. By the change of the composition in the aforementioned manner, the n-type clad layer 44 lattice-matched with the buffer layer 3 in a face touching the buffer layer 3
15 and lattice-matched with the light-emitting layer 5 in a face touching the light-emitting layer 5 is obtained. As a result, the n-type clad layer 44 and the light-emitting layer 5 are formed on lattice-matched undercoats respectively, so that the crystallinity of the light-emitting layer 5 is improved
20 synergistically.

Further, in the face touching the light-emitting layer 5, the band gap of the n-type clad layer 44 is wider than the band gap of the light-emitting layer 5, so that the n-type clad layer 44 has the role of a barrier layer to holes generated in
25 the light-emitting layer 5.

When the MOCVD method is used for the formation of the n-type clad layer 44, the composition ratio of raw-material gases is changed continuously. In this manner, the n-type clad

layer 44 having the composition changed continuously in the direction toward the light-emitting layer 5 side from the buffer layer 3 side is obtained.

SIXTH EMBODIMENT

5 Fig. 6 shows an enlarged view of important part of a light-emitting diode 50 as a further embodiment of the present invention. Incidentally, the same members as used in the light-emitting diode 1 in the first embodiment are referred to by the same characters and the description thereof will be
10 omitted.

In the light-emitting diode 50, the composition of an n-type clad layer 54 is changed to three stages of n-Al_{0.34}Ga_{0.33}In_{0.33}N (doped with Si), n-Al_{0.22}Ga_{0.48}In_{0.30}N (doped with Si) and n-Al_{0.11}Ga_{0.61}In_{0.28}N (doped with Si) in the direction toward
15 the light-emitting layer 5 side from the buffer layer 3 side. By the change of the composition in the aforementioned manner, the n-type clad layer 54 lattice-matched with the buffer layer 3 in a face touching the buffer layer 3 and lattice-matched with the light-emitting layer 5 in a face touching the light-emitting
20 layer 5 is obtained. As a result, the n-type clad layer 54 and the light-emitting layer 5 are formed on lattice-matched undercoats respectively, so that the crystallinity of the light-emitting layer 5 is improved synergistically.

Further, in the face touching the light-emitting layer
25 5, the band gap of the n-type clad layer 54 is wider than the band gap of the light-emitting layer 5, so that the n-type clad layer 54 has the role of a barrier layer to holes overflowed from the light-emitting layer 5.

When the MOCVD method is used for the formation of the n-type clad layer 54, the composition ratio of raw-material gases is changed stepwise. In this manner, the n-type clad layer 54 having the composition changed stepwise in the direction toward the light-emitting layer 5 side from the buffer layer 3 side is obtained.

Although this embodiment has shown the case where the n-type clad layer is changed to three stages, the present invention is not limited to the three-stage change.

This invention is not limited to the above description of the mode for carrying out the invention and embodiments thereof at all, and includes various modifications that can be conceived by those skilled in the art without departing from the scope of the claims.

The following facts will be disclosed below.

A group III nitride compound semiconductor device of a successively laminated structure comprising:

a substrate;

a buffer layer;

a first layer formed of doped $In_xGa_{1-x}N$ ($0 < x < 1$); and

a second layer formed of non-doped $In_yGa_{1-y}N$ ($0 < y < 1$).

In the above semiconductor device, the composition ratio of In in the first layer is changed continuously or intermittently in the direction toward the second layer side from the buffer layer side so that the composition of the first layer in a face touching the second layer becomes substantially equal to the composition of the second layer.

WHAT IS CLAIMED IS:

1. A group III nitride compound semiconductor device
of a successively laminated structure comprising:

a substrate;

5 a buffer layer;

a first layer formed of $In_xGa_{1-x}N$ ($0 < x < 1$); and

a second layer formed of $In_yGa_{1-y}N$ ($0 < y < 1$, $y \neq x$).

2. A group III nitride compound semiconductor device
10 according to claim 1, wherein a composition ratio of In in said
first layer is changed continuously or intermittently in a
direction toward the second layer side from the buffer layer
side so that a composition of said first layer in a face brought
into contact with said second layer becomes substantially equal
15 to a composition of said second layer.

3. A group III nitride compound semiconductor device
of a successively laminated structure comprising:

a substrate;

20 a buffer layer;

a first layer formed of $Al_aGa_bIn_{1-a-b}N$ ($0 < a < 1$, $0 < b < 1$,
 $a+b < 1$); and

a second layer formed of $In_yGa_{1-y}N$ ($0 < y < 1$).

25 4. A group III nitride compound semiconductor device
according to claim 3, wherein a composition ratio of Al and In
in said first layer is changed continuously or intermittently
in a direction toward the second layer side from the buffer layer

side so that a lattice constant of said first layer in a face brought into contact with said second layer becomes substantially equal to a lattice constant of said second layer.

5 5. A group III nitride compound semiconductor device according to claim 3, wherein a composition ratio of Al and In in said first layer is changed continuously or intermittently in a direction toward the second layer side from the buffer layer side so that a band gap of said first layer in the face brought
10 into contact with said second layer becomes wider than a band gap of said second layer.

6. 6. A group III nitride compound semiconductor device according to claim 4, wherein the composition ratio of Al and
15 In in said first layer is changed continuously or intermittently in the direction toward the second layer side from the buffer layer side so that a band gap of said first layer in a face brought into contact with said second layer becomes wider than a band gap of said second layer.

ABSTRACT OF THE DISCLOSURE

An InGaN layer is formed on an undercoat layer of the same composition as the InGaN layer. The composition of the undercoat layer may be changed continuously or stepwise.

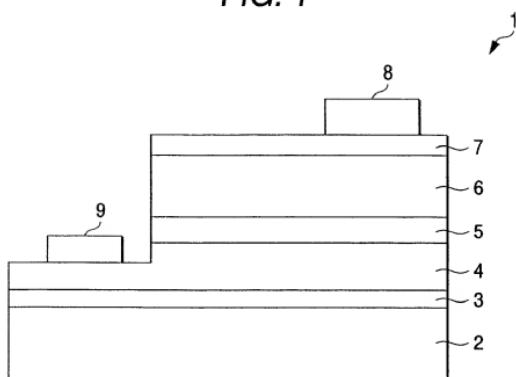
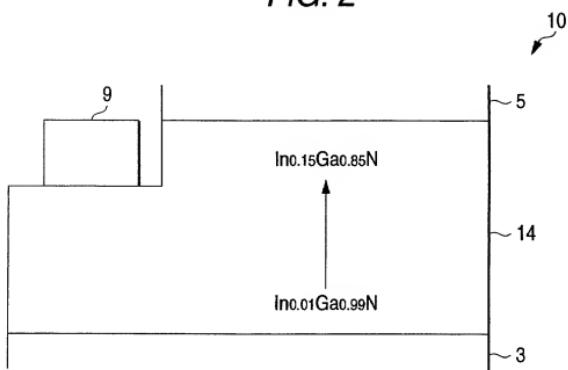
FIG. 1*FIG. 2*

FIG. 3

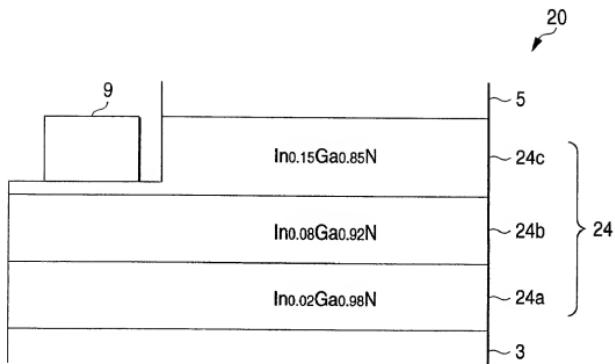


FIG. 4

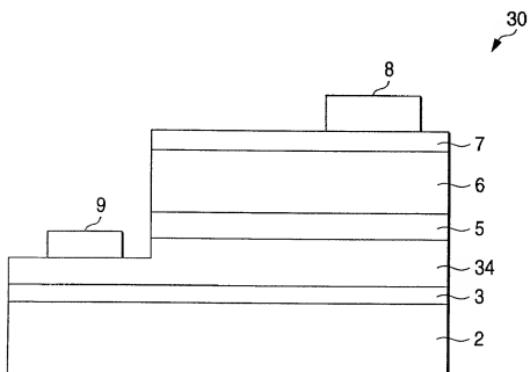


FIG. 5

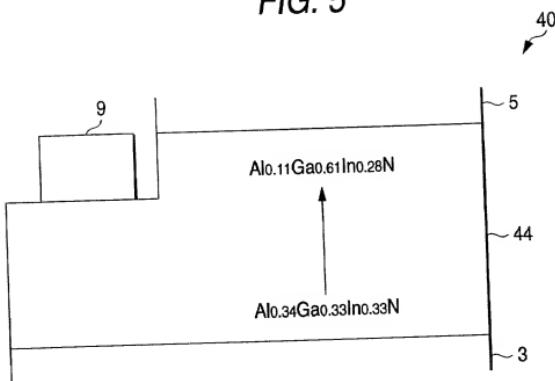
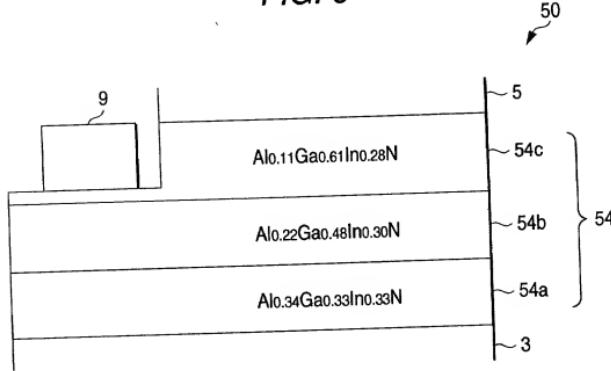


FIG. 6



As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name, and I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the INVENTION ENTITLED
GROUP III NITRIDE COMPOUND SEMICONDUCTOR DEVICE

the specification of which (**CHECK** applicable **BOX(ES)**)

-> [X] is attached hereto.

-> [] was filed on _____ as U.S. Application No. 0 /
BOX(ES) -> [] was filed as PCT International Application No. PCT/ / on

-> -> and (if applicable to U.S. or PCT application) was amended on _____
I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose all information known to me to be material to patentability as defined in 37 C.F.R. 1.56. I hereby claim foreign priority benefits under 35 U.S.C.119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate filed by me or my assignee disclosing the subject matter claimed in this application and having a filing date (1) before that of the application on which priority is claimed, or (2) if no priority claimed, before the filing date of this application:

PRIOR FOREIGN APPLICATION(S)	Date first Laid-open or Published	Date Patented or Granted	Priority Claimed
Number Country P. Hei. 11-065880 Japan	Day/Month/Year Filed 12/March/1999		Yes X No

I hereby claim domestic priority benefit under 35 U.S.C.120/365 of the indicated United States applications listed below and PCT international applications listed above or below and, if this is a continuation-in-part (CIP) application, insofar as the subject matter disclosed and claimed in this application is in addition to that disclosed in such prior applications, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in 37 C.F.R. 1.56 which became available between the filing date of each such prior application and the national or PCT international filing date of this application:

PRIOR U.S. PROVISIONAL, NONPROVISIONAL AND/OR PCT APPLICATION(S)	Status	Priority Claimed
Application No. (series code/serial no.) Day/Month/Year Filed	pending, abandoned, patented	Yes No

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

And I hereby appoint Cushman Darby & Cushman Intellectual Property Group of Pillsbury Madison & Sutro LLP, 1100 New York Avenue, N.W., Ninth Floor, East Tower, Washington, D.C. 20005-3918, telephone number (202) 861-3000 (to whom all communications are to be directed), and the below-named persons (of the same address) individually and collectively my attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith and with the resulting patent, and I hereby authorize them to delete names/numbers below of persons no longer with their firm and to act and rely on instructions from and communicate directly with the person/assignee/attorney/firm/organization who/which first sends/entitled this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct the above Firm and/or a below attorney in writing to the contrary.

Paul N. Kokulis	16773	David W. Brinkman	20817	Chris Comuntzis	31097	David A. Jakopin	32995
Raymond F. Lippitt	17519	George M. Stirlla	18221	Lawrence Harbin	27644	Mark G. Paulson	30793
G. Lloyd Knight	17698	Donald J. Bird	25232	Paul E. White, Jr.	32011	James D. Berquist	34776
Carl G. Love	18781	W. Warren Talavull	25647	Michelle N. Lester	32331	Timothy J. Klima	34852
Edgar H. Martin	20534	Peter W. Gowday	25872	Jeffrey A. Simenauer	31993	John P. Moran	30906
William K. West, Jr.	22057	Dale S. Lazar	28872	Robert A. Molan	29834	Stephen C. Glazier	31361
Kevin E. Joyce	20508	Glen J. Perry	28458	G. Paul Egell	24238	Paul F. McQuade	31542
Edward M. Prince	22429	Kendrew H. Colton	30368	Lynn E. Eccleston	35861		

1. INVENTOR'S SIGNATURE: *Naoki Shishibata* Date January 20, 2000
Inventor's Name (typed) Naoki Shishibata Country of Citizenship Japan
Residence (City) Bisai-shi First Middle Initial F Family Name Aichi, Japan

Post Office Address (Include Zip Code) 18-4, Iriinishikuruwa, Kaimei, Bisai-shi, Aichi, Japan

2. INVENTOR'S SIGNATURE: _____ Date _____
Inventor's Name (typed) _____ First Middle Initial _____ Family Name _____ Country of Citizenship _____
Residence (City) _____ (State/Foreign Country) _____

Post Office Address (Include Zip Code) _____

3. INVENTOR'S SIGNATURE: _____ Date _____
Inventor's Name (typed) _____ First Middle Initial _____ Family Name _____ Country of Citizenship _____
Residence (City) _____ (State/Foreign Country) _____

Post Office Address (Include Zip Code) _____

(FOR ADDITIONAL INVENTORS, check box [] and attach sheet (CDC-116.2) for same information for each re signature, name, date, citizenship, residence and address.)

Rule 56(a) & (b) = 37 C.F.R.1.56(a) & (b)
PATENT AND TRADEMARK CASES - RULES OF PRACTICE
DUTY OF DISCLOSURE

(a) ...Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the [Patent and Trademark] Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability... (b) information is material to patentability when it is not cumulative and (1) It also establishes by itself, or in combination with other information, a prima facie case of unpatentability of a claim or (2) refers, or is inconsistent with, a position the applicant takes in: (i) Opposing an argument of unpatentability relied on by the Office, or (ii) Asserting an argument of patentability.

PATENT LAWS 35 U.S.C.

§102. Conditions for patentability; novelty and loss of right to patent

A person shall be entitled to a patent unless--

- (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for patent or
- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States, or
- (c) he has abandoned the invention, or
- (d) the invention was first patented or caused to be patented, or was the subject of an inventor's certificate, by the applicant or his legal representatives or assigns in a foreign country prior to the date of the application for patent in this country on an application for patent or inventor's certificate filed more than twelve months* before the filing of the application in the United States, or
- (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent, or
- (f) he did not himself invent the subject matter sought to be patented, or
- (g) before the applicant's invention thereof the invention was made in this country by another who had not abandoned, suppressed, or concealed it. In determining priority of invention there shall be considered not only the respective dates of conception and reduction to practice of the invention, but also the reasonable diligence of one who was first to conceive and last to reduce to practice, from a time prior to conception by the other.

§103. Condition for patentability; non-obvious subject matter

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made. Subject matter developed by another person, which qualified as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

* Six months for Design Applications (35 U.S.C. 172).